CMOS IMAGE SENSOR HAVING ROW DECODER CAPABLE OF SHUTTER TIMING CONTROL

ABSTRACT OF THE DISCLOSURE

The present invention relates to a CMOS image sensor having a row decoder capable of shutter timing control, the row decoder addressing to a plurality of pixels arranged in rows and columns in a CMOS image sensor and including a plurality of unit arrays, wherein the unit arrays include a first NAND gate for generating a reset gate signal in response to an address signal and a reset signal, a second NAND gate for generating a selection gate signal in response to the address signal and a selection signal, a latch for resetting an output thereof in response to an address latch signal and latching the address signal as the output in response to the address latch signal and the address signal, a third NAND gate for receiving the address signal and a transmitted signal, a fourth NAND gate for receiving the output of the latch and a shutter transmitted signal, and an OR gate for receiving the outputs of the third and fourth NAND gates and generating a transmitted gate signal; wherein shuttering of a row address is latched in accordance with the blank interval of the horizontal synchronization signal using latches of the row decoder, and the shuttering operation is performed sequentially increasing the shuttering row address by 1, the invalid data that are not shuttered are thereby prevented from being generated though the row shutter value is changed suddenly.